Development of a transistor compact model to increase the design accuracy of 'system semiconductor'

— Professor Sung-Min Hong's team solves the difficulties in the transistor model development process and improves model accuracy

▲ From left: Professor Sung-Min Hong and Ph.D. student Kwang-Woon Lee

A research team at GIST (Gwangju Institute of Science and Technology, President Kiseon Kim) succeeded in lowering the maximum error of the transistor compact model* essential for circuit design to less than 6% in the field of system semiconductor**, which is attracting attention as a future investment destination for the domestic semiconductor industry.

If the accuracy of the compact model is improved as a result of this research, it is expected that the accuracy of the system semiconductor design can be improved by reducing the error due to the limitations of the compact model.

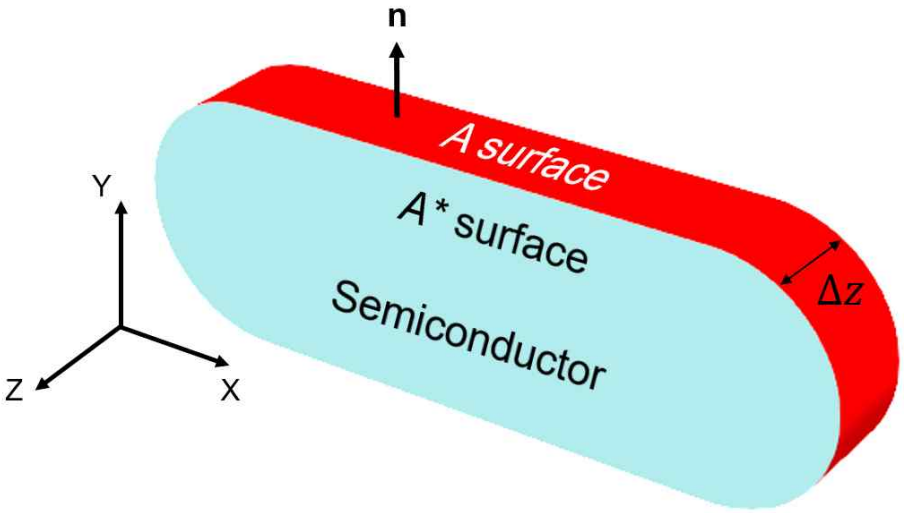
* **compact model:** A model that expresses the current-voltage characteristics of the transistors composing the circuit with a simple (compact) formula. As it is used in the SPICE program that calculates the electrical characteristics of the circuit, it is an essential model in circuit design.

** **system semiconductor:** A semiconductor with information processing functions such as arithmetic and control. Samsung Electronics announced (2019) that it will invest 133 trillion won in R&D and production facilities expansion in the system semiconductor field by 2030 and hire 15,000 professionals.

As the time from order to final delivery continues to increase due to global semiconductor shortages, accurate transistor compact models are essential for design accuracy, especially in the field of system semiconductors.

In the meantime, the cross-sectional shape of the transistor, which varies depending on the process and design, is acting as a limit to the development of a universal compact model. In addition, existing models such as BSIM*, which have been used by semiconductor manufacturers around the world, have limitations in applying them to the latest transistors with complex cross-sectional structures.

* **Berkeley Short-channel IGFET Model (BSIM):** a transistor compact model developed by the BSIM group at UC Berkeley, which is one of the most widely used compact models today



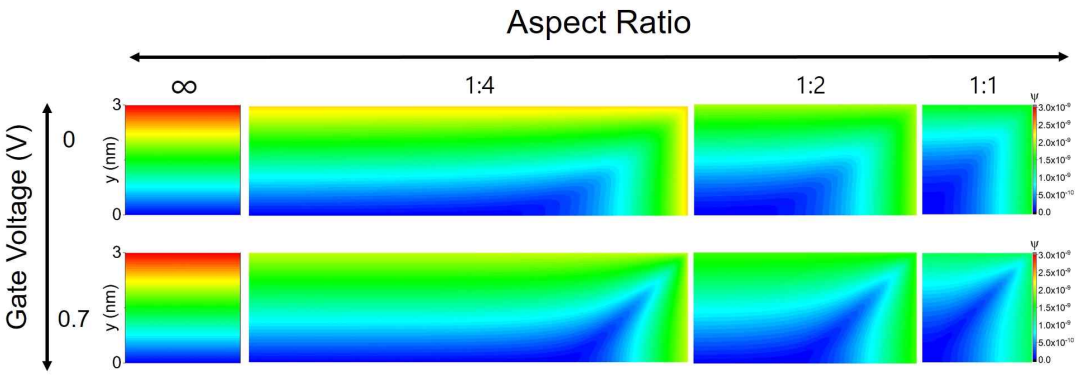
▲ The cross-sectional shape of the transistor. Transistors have different cross-sectional shapes on the xy plane (a light blue rectangle with rounded corners in this figure) depending on the process and design, so it has been considered a challenge to develop a universal compact model that can be applied to any cross-section.

Existing compact models use approximate relations obtained inductively from simple sections, and errors caused by inaccurate models are reduced by fine-tuning model parameters. This process requires a lot of time and manpower.

GIST School of Electrical Engineering and Computer Science Professor Sung-Min Hong's research team derived a universal compact model that can be applied to any transistor cross section.

The research team found that even if the cross-sectional shape of the transistor is different, the amount of charge depending on the gate voltage approximates the empirical relation. Based on this fact, they succeeded in lowering the maximum error of the calculation result to less than 6% by deriving a universal relational expression that can be applied to any transistor cross-section.

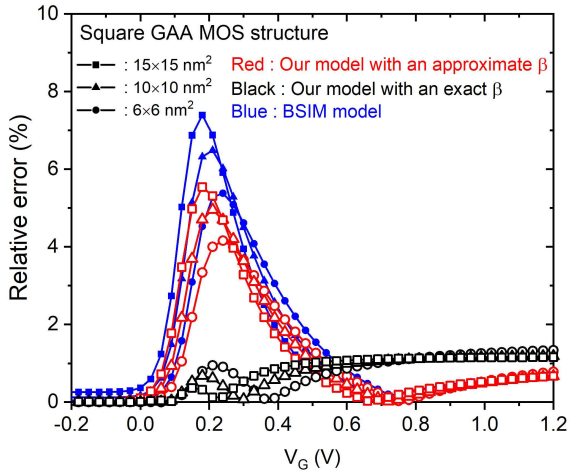
The research team generated generalized coordinates suitable for the cross section of the transistor and calculated a weighting factor from these coordinates. In the subsequent compact model development process, this weight was used to derive a universal compact model that holds regardless of the cross-sectional shape. The parameters used in the derived compact model can be easily calculated from a given cross section, so there is no need for additional fine-tuning.



▲ Calculated generalized coordinates for rectangular sections. It can be seen that the generalized coordinates are also changed when changing the ratio of the width and length of the rectangle. Since information about the cross-sectional shape is reflected in the generalized coordinates, it is possible to develop a universal compact model using these coordinates.

Comparing the derived universal compact model and the empirical relation used in the existing model, it can be seen that the overall form is similar but that the coefficients of each term are different, and this difference causes a difference in the calculation results. The universal compact model derived from all the considered cross-sectional shapes showed improved accuracy than the conventional model.

Professor Sung-Min Hong said, "The results of this study are of greatest significance because the induction process of the compact model is clearly clarified and the accuracy is improved, and this is expected to contribute on research to connect semiconductor device simulation and compact model in the future."



▲ The error of the compact model for square sections. The square cross section is the case where the largest error occurs. The presented universal compact model (black) is much more accurate than the conventional model (blue). Even when an approximation is introduced (red) to facilitate the calculation of parameters used in the model, it is superior in accuracy compared to the existing model.

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